WHAT IS CLAIMED IS:

1. A method of determining a fail string for a device comprising the steps of:

determining a test pattern for a portion of an address space wherein the test pattern includes at least one address in the address space and the portion of the address space includes at least one x address and at least one y addresses;

executing a test a plurality of times for each test pattern, wherein every combination of the test pattern is tested, wherein the combinations include each address held at a first potential for at least a first test and a second potential for at least a second test;

determining a fail string for the device including pass/fail results for the test pattern; and

combining the pass/fail results in the fail string.

2. The method of claim 1, wherein the portion of the address space to be tested corresponds to a number of addresses comprising each test pattern.

3. The method of claim 1, wherein the test pattern includes a single address.

4. The method of claim 3, further comprising the steps of:

holding the test pattern at the first potential during a first test, yielding in a pass/fail result; and

holding the test pattern at the second potential during a second test, yielding in a pass/fail result.

5. The method of claim 1, further comprising the step of executing the test for the test pattern, wherein the test pattern is a combination of at least one address.

6. The method of claim 1, wherein the step of determining the test pattern further includes the step of determining at least one x address and at least one y address according to a targeted fail type, wherein the targeted fail type is identified using a subset of the addresses in the address space.

7. The method of claim 1, further comprising the step of generating a pseudo compressed bitmap comprising a plurality of cells, wherein each cell is one of a passing cell and a failing cell.

8. The method of claim 7, wherein the failing cell manifests itself as a fail in the pass/fail results for every test pattern and the passing cell has at least one pass result for at least one test pattern.

9. The method of claim 1, further comprising the step of generating a pareto.

10. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating a pseudo compressed bitmap for a device, the method steps comprising:

determining a test pattern for a portion of an address space wherein the test pattern includes at least one address in the address space and the portion of the address space includes at least one x address and at least one y addresses;

executing a test a plurality of times for each test pattern, wherein every combination of the test pattern is tested, wherein the combinations include each address held at a first potential for at least a first test and a second potential for at least a second test;

determining a fail string for the device including pass/fail results for the test pattern; and

generating a pseudo compressed bitmap by combining each pass/fail result according to a Boolean AND function.

11. The method of claim 10, wherein the portion of the address space to be tested corresponds to a number of addresses comprising each test pattern.

12. The method of claim 10, wherein the test pattern includes a single address.

13. The method of claim 12, further comprising the steps of:

holding the test pattern at the first potential during a first test, yielding in a pass/fail result; and

holding the test pattern at the second potential during a second test, yielding in a pass/fail result.

14. The method of claim 10, further comprising the step of executing the test for the test pattern, wherein the test pattern is a combination of at least one address.

15. The method of claim 10, wherein the step of determining the test pattern further includes the step of determining at least one x address and at least one y address according to a targeted fail type, wherein the targeted fail type is identified using a subset of the addresses in the address space.

16. The method of claim 10, wherein the pseudo compressed bitmap comprises a plurality of cells, wherein each cell is one of a passing cell and a failing cell.

17. The method of claim 16, wherein the failing cell manifests itself as a fail in the pass/fail results for every test pattern and the passing cell has at least one pass result for at least one test pattern.

18. A method of generating a pseudo compressed bitmap for a device comprising the steps of:

generating a pseudo compressed bitmap by combining a plurality of pass/fail results according to a Boolean AND function;

displaying the pseudo compressed bitmap wherein the pass/fail results correspond to at least one X address pin and one Y address pin, and wherein each address pin corresponds to a plurality of pass/fail results.

19. The method of claim 18, wherein every combination of a test pattern including at least one address is tested, wherein the combinations include each address held at a first potential for at least a first test and a second potential for at least a second test.